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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/273,784	03/22/1999	JOHN G. MCBRIDE	10971308-1	7570

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EXAMINER
PHAN, THAI Q

ART UNIT	PAPER NUMBER
2123	

DATE MAILED: 04/24/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/273,784	Applicant(s) John McBride
	Examiner Thai Phan	Art Unit 2123

-- Th MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on Jan. 30, 2002

2a) ☒ This action is **FINAL.** 2b) ☐ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) 1-20 is/are pending in the applica

4a) Of the above, claim(s) _____ is/are withdrawn from considera

5) ☐ Claim(s) _____ is/are allowed.

6) ☒ Claim(s) 1-20 is/are rejected.

7) ☐ Claim(s) _____ is/are objected to.

8) ☐ Claims _____ are subject to restriction and/or election requirem

Application Papers

9) ☐ The specification is objected to by the Examiner.

10) ☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved.

12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

13) ☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

a) ☐ All b) ☐ Some* c) ☐ None of:

1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

*See the attached detailed Office action for a list of the certified copies not received.

14) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

15) ☐ Notice of References Cited (PTO-892)

16) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

17) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s). _____

18) ☐ Interview Summary (PTO-413) Paper No(s). _____

19) ☐ Notice of Informal Patent Application (PTO-152)

20) ☐ Other:

DETAILED ACTION

This Office Action is responsive to applicant's response filed Jan. 30, 2002. Claims 1-20 are pending in this official action.

Claim Rejections - 35 USC § 101

1. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

2. Claims 15-20 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. Claims 15-20 are directed to data on a disk, which comprises code or set of instructions with limitation features (see claim 15). The claimed computer program per se or instruction code with feature represented for analysis of transistor gate for noise immunity as claimed is not a statutory subject matter because it is directed to a data structure. It is necessarily to be converted into executable code and executed by a computer to meet statutory requirement.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371© of this title before the invention thereof by the applicant for patent.

4. Claims 1-20 are rejected under 35 U.S.C. 102(b) as being anticipated by Ikeda et al., patent no. 5,446,674.

As per claims 1 and 15, Ikeda anticipated method and operation system for checking design rule as claimed. According to Ikeda, the method and system for design rule checker includes a computer configured to execute a rule checker program, wherein the design rule being checked for an integrated circuit design having gates, gate connected in datapath or along circuit paths including static gate characteristics, transistor parameters such as transistor widths, lengths, connected in device channel, etc. ("Summary of the Invention", col. 1, line 44 to col. 2, line 24, col. 2, lines 24-53, col. 5, lines 18-56, col. 9, line 45 to col. 10, line 10). The program is designed to check transistor susceptible to noise in the cross-talk influence (col. 2, lines 7-24, col. 5, lines 18-56, col. 9, line 54 to col. 10, line 2), including checking noise susceptible or noise immunity as claimed for transistors to other transistors as claimed because they are parts of noise control scheme.

As per claim 2, Ikeda anticipated reading transistor design parameters for design rule check as claimed. Such transistor circuit design would include for example inverter gate, p-channel and n-channel transistor, CMOS channel parameters, design parameters, etc. as well-known in transistor circuit design.

As per claims 3-7, the rule checker program as in the art of record obtains transistor design parameters or extracting the design parameters as claimed, and checks with the operating conditions as claimed ("Summary of the Invention").

As per claim 8, Ikeda anticipated the method for checking design rule including checking transistor design parameters in compatible with different operating conditions or with different transistor layout configuration such that susceptible noise would be checked for high power voltage, heat generation, different transistor threshold, etc. According to Ikeda, the method and system for design rule checker includes a computer configured to execute a rule checker program, wherein the design rule being checked for an integrated circuit design having gates, gate connected in datapath or along circuit paths including static gate characteristics, transistor parameters such as transistor widths, lengths, connected in device channel, etc. ("Summary of the Invention", col. 1, line 44 to col. 2, line 24, col. 2, lines 24-53, col. 5, lines 18-56, col. 9, line 45 to col. 10, line 10). The program is designed to check transistor susceptible to noise in the cross-talk influence (col. 2, lines 7-24, col. 5, lines 18-56, col. 9, line 54 to col. 10, line 2), including checking noise susceptible or noise immunity as claimed for transistors to other transistors as claimed because they are parts of noise control scheme.

As per claims 9-14, due to the similarity of claims 9-14 to claims 2-7; therefore claims 9-14 are also rejected in like manner.

Similarly, claims 16-20 are also rejected under the same rationales as above because the claims are directed to computer program codes, when executed (hopefully), for performing steps

of rule check, and controlling an apparatus for performing steps of method claims as in claims 2-7 and in claims 9-14.

Response to Arguments

5. Applicant's arguments with respect to claims 1-20 have been considered but are not persuasive.

In response to applicant's argument claims 15-20 are directed to a statutory subject matter (page 3, last paragraph), the examiner disagrees with. Claims 15-20, especially claim 15, are directed to a non-statutory subject matter because the claims 15-20 are directed to a computer program per se, which comprises code or set of instructions on a medium which analyzes the width of the field effect transistors to determine whether or not the gate has an acceptable noise immunity (see claim 15). Computer program per se or instruction code (raw) in a medium as claimed is not a statutory subject matter because it is not functionally transformed or converted into a useful product effectively to carry out practically useful application to meet statu requirement.

In response to applicant's argument Ikeda disclosure failed to teach limitations as cited in claim 1 (see page 5), the examiner disagrees with. Ikeda anticipated method and system for verifying cross-talk or noise generated in an integrated circuit device ("Summary of the Invention"), or analyzing gate transistor susceptible to noise (col. 2, lines 24-53, col. 5, lines 18-56, col. 9, line 45 to col. 10, line 20).

In response to applicant's argument Ikeda failed to teach cross-talk noise immunity by analysis of widths of field effect transistors (page 6, paragraphs 4-5), the examiners disagrees with. Ikeda anticipated cross-talk noise influence and transistor susceptible to cross-talk by analyzing transistror (FET)device parameters such as widths, lengths, and sizes (col. 9, line 45 to col. 10, line 10).

In response to applicant's argument Ikeda failed to analyze the width of the FET in the computer to determine whether or not the gate has an acceptable noise immunity, wherein the computer executes a rule checker program which analyzes the widths to determine ... acceptable noise immunity (page 8), the examiner disagrees with. Ikeda anticipated the method for checking design rule including checking transistor design parameters in compatible with different operating conditions or with different transistor layout configuration such that susceptible noise would be checked for high power voltage, heat generation, different transistor threshold, etc. According to Ikeda, the method and system for design rule checker includes a computer configured to execute a rule checker program, wherein the design rule being checked for an integrated circuit design having gates, gate connected in datapath or along circuit paths including static gate characteristics, transistor parameters such as transistor widths, lengths, transistor sizes, including W/L, connected in device channel, etc. ("Summary of the Invention", col. 1, line 44 to col. 2, line 24, col. 2, lines 24-53, col. 5, lines 18-56, col. 9, line 45 to col. 10, line 10). The program is designed to check transistor susceptible to noise in the cross-talk influence (col. 2, lines 7-24, col.

5, lines 18-56, col. 9, line 54 to col. 10, line 2), including checking noise susceptible or noise immunity as claimed for transistors influenced by noise.

Conclusion

6. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thai Phan whose telephone number is (703) 305-3812.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703)305-3900.

Any response to this final action should be mailed to:

Box AF

Commissioner of Patents and Trademarks

Washington, D.C. 20231

or faxed to:

(703) 746-7238, (for formal communications; please mark "EXPEDITED PROCEDURE"),

Or:

(703) 746-7240 (for informal or draft communications, please label "PROPOSED" or "DRAFT")

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington. VA., Sixth Floor (Receptionist).

April 3, 2002

KEVIN J. TESKA
SUPERVISORY
PATENT EXAMINER